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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/686,701	10/17/2003	Takanaga Yamazaki	XA-9955	8811

181 7590 06/16/2006

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EXAMINER	
ZALEPA, GEORGE D	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 06/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/686,701	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	George D. Zalepa	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/17/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-14 have been considered by the examiner.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file:

a. Declaration as filed on 10/17/2003.

Information Disclosure Statement

3. The references listed in the Information Disclosure Statement submitted on 10/17/2003 have been considered by the examiner (see attached PTO-1449).

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Data processor able to transfer the contents of multiple registers to and from memory utilizing one instruction.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-15 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 1, 7-10, and 11 recite the limitation "numbers equal to or greater than, or equal to or smaller than a number" which encompasses an infinite number of values, thus rendering the claim indefinite.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-2, 4-5, 7-11 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Kahle et al. (US Pat. No. 5,694,565; herein referred to as "Kahle").

9. Regarding **independent claim 1**,

10. Kahle discloses *a data processor including a plurality of registers usable for instruction execution* [see Kahle, Fig. 1, element 32] *and having an instruction set including a plurality of predetermined data transfer instructions* [see Kahle, Col. 1, lines 52-54; Col. 2, lines 3-5], *wherein the predetermined data transfer instructions include a register specification field of plural bits in which the number of one register is explicitly specified from a group of registers* [see Kahle, Col. 5, lines 1-5; Examiner's note: register "r28" is considered the specification field, as it designates a starting address. Similarly in Col. 6, lines 12-15, register "r3" is considered to be the specification field.], *and wherein the predetermined data transfer instructions specify data transfers between registers corresponding to numbers equal to or greater than, or equal to or smaller than a number specified in the register specification field and memory* [see Kahle, Col. 5, lines 1-5; Examiner's note: To clarify, if the specification field contained "r28" as in col. 5, 4 register values would be loaded from memory thus a number smaller than the number specified in the specification thus a number loaded/stored less than the specification. However, if the specification was, for example, "r3" (as in Col. 6, lines 12-15), the instruction would load/store 29 instructions thus a number loaded/stored greater than the specification. Finally, if the specification was "r16" the instruction would load/store 16 instructions, thus an equal number.]

11. Regarding **claim 2**,

12. Kahle discloses the data processor according to claim 1, wherein the group of registers includes general purpose registers [see Kahle, Col. 3, lines 21-25; "general purpose registers"].

13. Regarding **claim 4**,

14. Kahle discloses *the data processor according to claim 1, wherein the predetermined data transfer instructions include register indirectly addressing mode, and wherein a register used in the register indirectly addressing mode is incremented or decremented for each transfer between the register and memory* [see Kahle, Col. 6, lines 12-15; Examiner's note: In this citation Kahle discloses utilizing register values to determine the memory location to store data to (note: the process is similar in a load instruction). Inherently, in a multiple store/load instruction, the memory location would have to be incremented to update the memory location being written to or from, thus incrementing the register values for each load/store.].

15. Regarding **claim 5**,

16. Kahle does not explicitly disclose *a register used in the register indirectly addressing mode is a stack pointer.* However, the use of multiple load and store instructions is primarily for stack operations as can be seen in the attached documentation on the ARM7TDMI-S processor (page 1-11, "Multiple Block Data Operations"). The use of the load/store multiple instructions is utilized for stack operations as it is a simple instruction to move a large amount of data that eventually must be moved to memory during a subroutine or the like. Thus, it would have been inherent that a stack pointer would be used during a load/store multiple instruction. Furthermore, in US Pat. 5,574,873 to Davidian, Davidian uses a multiple move instruction in a return from subroutine routine (Col. 7, lines 21-28), thus further showing the use of multiple load/store instructions in relation to stack operations. Furthermore, Davidian shows the use of a stack pointer stored in a general purpose register (Col. 10, line 50 "r1 a7"; Col. 12, lines 25-27) within the same architecture (POWER) as Kahle.

17. Regarding **claim 7**,

18. Kahle discloses *the data processor according to claim 1, wherein the predetermined data transfer instructions include a first store instruction* [see Kahle, Col. 6, lines 8-10 "store multiple instruction".] *specifying data transfers to memory from registers corresponding to numbers equal to or greater than a number specified in a register specification field as a starting point* [see Kahle, Col. 5, lines 1-5; Col. 6, lines 13-16; Examiner's note: To clarify, if the specification was, for example, "r3" (as in Col. 6, lines 12-15), the instruction would load/store 29 instructions thus a number loaded/stored greater than the specification. Finally, if the specification was "r16" the instruction would load/store 16 instructions, thus an equal number. Furthermore, it is clear from the col. 5 and col. 6 cites that this principle applies to both load and store instructions.].

19. Regarding **claim 8**,

20. Kahle discloses *the data processor according to claim 1, wherein the predetermined data transfer instructions include a first load instruction* [see Kahle, Col. 5, lines 1-5] *specifying data transfers from memory to registers corresponding to numbers equal to or greater than a number specified in a register specification field as a starting point* [see Kahle, Col. 5, lines 1-5; Examiner's note: register "r28" is considered the specification field, as it designates a starting address. Similarly in Col. 6, lines 12-15, register "r3" is considered to be the specification field.], *and wherein the predetermined data transfer instructions specify data transfers between registers corresponding to numbers equal to or greater than, or equal to or smaller than a number specified in the register specification field and memory* [see Kahle, Col. 5, lines 1-5; Examiner's note: To clarify, if the specification was, for example, "r3" (as in Col. 6, lines 12-15), the instruction would load/store 29 instructions thus a number loaded/stored greater than the specification. Finally, if the specification was "r16" the instruction would load/store 16

instructions, thus an equal number. Furthermore, it is clear from the col. 5 and col. 6 cites that this principle applies to both load and store instructions.].

21. Regarding **claim 9**,

22. Kahle discloses *the predetermined data transfer instructions include a second store instruction* [see Kahle, Col. 6, lines 8-10] *specifying data transfers to memory from registers corresponding to numbers equal to or smaller than a number specified in a register specification field as a starting point* [see Kahle, Col. 5, lines 1-5; Examiner's note: register "r28" is considered the specification field, as it designates a starting address. Similarly in Col. 6, lines 12-15, register "r3" is considered to be the specification field.], *and wherein the predetermined data transfer instructions specify data transfers between registers corresponding to numbers equal to or greater than, or equal to or smaller than a number specified in the register specification field and memory* [see Kahle, Col. 5, lines 1-5; Examiner's note: To clarify, if the specification field contained "r28" as in col. 5, 4 register values would be loaded from memory thus a number smaller than the number specified in the specification thus a number loaded/stored less than the specification. If the specification was "r16" the instruction would load/store 16 instructions, thus an equal number. Furthermore, it is clear from the col. 5 and col. 6 cites that this principle applies to both load and store instructions.].

23. Regarding **claim 10**,

24. Kahle discloses *the predetermined data transfer instructions include a second load instruction* [see Kahle, Col. 5, lines 1-5] *specifying data transfers from memory to registers corresponding to numbers equal to or smaller than a number specified in a register specification field as a starting point* [see Kahle, Col. 5, lines 1-5; Examiner's note: To clarify, if the specification field contained "r28" as in col. 5, 4 register values would be loaded from memory thus a number smaller than the number specified in the specification thus a number loaded/stored less than the specification. If the specification was "r16" the instruction would load/store 16 instructions,

thus an equal number. Furthermore, it is clear from the col. 5 and col. 6 cites that this principle applies to both load and store instructions.].

25. Regarding **independent claim 11**,

26. Kahle discloses *a data processor including an instruction control part for decoding* [see Kahle, Col.3, lines 50-53; "dispatch/decode"] *instructions and controlling instruction execution sequences* [see Kahle, Fig. 1, elements 14, 17-20; Examiner's note: The elements listed are considered to act as a controlling element as they perform control functions as opposed to the execution units.], *and a plurality of registers* [see Kahle, Fig. 1, element 32], *wherein the instruction control part, when decoding a number specified in a register specification field of plural bits paired with specific operation code, controls data transfers between a group of registers* [see Kahle, Col. 4, lines 38-44; Examiner's note: Description of dispatch (decode) or multiple load instruction, inherently the same process for multiple store instructions.] *corresponding to numbers equal to or greater than, or equal to or smaller than the number, and memory* [see Kahle, Col. 5, lines 1-5; Examiner's note: To clarify, if the specification field contained "r28" as in col. 5, 4 register values would be loaded from memory thus a number smaller than the number specified in the specification thus a number loaded/stored less than the specification. However, if the specification was, for example, "r3" (as in Col. 6, lines 12-15), the instruction would load/store 29 instructions thus a number loaded/stored greater than the specification. Finally, if the specification was "r16" the instruction would load/store 16 instructions, thus an equal number.]

27. Regarding **claim 13**,

28. Kahle discloses *the data processor according to claim 11, wherein a group of registers specifiable by numbers of the register specification field includes general purpose registers* [see Kahle, Col. 3, lines 21-25; "general purpose registers"].

29. Claims 11-12 are rejected under 35 U.S.C. 102(b) as being anticipated by ARM ("ARM7TDMI-S Technical Reference Manual", ARM Limited, 2001).

30. Examiner's note: The Technical Reference Manual illustrates load multiple and store multiple instructions (Page 1-11, "Multiple Block Data Operations" (LDM); Page 1-12, "Store – Block Data Operations" (STM). However, document "ARM7 Data Sheet" ("ARM Data Sheet", ARM Limited, Dec 2004) provides a clearer explanation of the LDM and STM instructions utilized by the ARM7TDMI and is utilized to provide clearer explanation. "ARM7 Data Sheet" will herein be referred to as "ARM2".

31. Regarding **independent claim 11**,

32. ARM discloses *a data processor including an instruction control part for decoding instructions and controlling instruction execution sequences* [see ARM, Page 1-7, element "Instruction Decoder and Control Logic"], *and a plurality of registers* [see ARM, Page 1-7, element "Register Bank"], *wherein the instruction control part, when decoding a number specified in a register specification field* [see ARM2, Page 42, element "Register List"; ARM, Page 1-11, "Multiple Block Data Operations", "<reglist>" in instructions.] *of plural bits paired with specific operation code* [see ARM2, Page 43, §4.8.1, lines 2-3], *controls data transfers between a group of registers corresponding to numbers equal to or greater than, or equal to or smaller than the number, and memory* [see ARM, Page 43, §4.8.1, lines 3-4; Examiner's note: lines 3-4 show the transfer of any subset of instructions. Furthermore, if the register list was to transfer only register 1, the value of the register list would be 0000000000000010_2 (2) therefore the number of registers transferred (1) would be less than the value of the reglist field.].

33. Regarding **claim 12**,

34. ARM does disclose *the instruction control part can change the correspondence between numbers specifiable in the register specification field and registers according to setting states of a control register* [see ARM, Page 2-17, section "T bit"; Page 2-14, Fig. 2-5; Examiner's

note: ARM discloses switching to a thumb state which would map the register list onto a smaller register file thus changing the correspondence of the register specification field.].

Claim Rejections - 35 USC § 103

35. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

36. Claims 3 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kahle in view of Davidian (US Pat. No. 5,574,873; herein referred to as "Davidian").

37. Regarding **claim 3**,

38. Kahle discloses the limitations as stated in **independent claim 1**.

39. Kahle does not explicitly disclose *the group of registers* [including] *a procedure register in which a return address from a subroutine is stored when the subroutine is called.*

40. Davidian does disclose *the group of registers* [including] *a procedure register in which a return address from a subroutine is stored when the subroutine is called* [see Davidian, Col. 25, lines 9-13].

41. The advantage of including a procedure register containing a subroutine return address in the group of registers that are transferred to and from memory would have been to store all relevant data upon moving contents into memory. This concept is particular poignant in stack-based subroutine handling in which a return address is pushed onto the stack and popped off to return the flow of execution. The POWER series of processors utilizes a stack to handle subroutine, so it would have been obvious to one of ordinary skill in the art at the time of invention to include a procedure register containing a return address for a subroutine in the group of registers moved by a load multiple or store multiple instruction, as said load and store multiple instructions are

most frequently used to push and pop multiple data elements from a stack, as shown in the rejection of claim 5. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize a procedure register containing the return address of a subroutine with the goal of maintaining coherency during stack pushes and pops.

42. Regarding **claim 14**,

43. Kahle discloses the limitations as stated in **claim 13**.

44. Kahle does not explicitly disclose special purpose registers.

45. Davidian discloses special purpose registers [see Davidian, Fig. 1, element 12; Col. 4, lines 9-13]

46. Kahle does not disclose special-purpose registers within the disclosure, however it would have been obvious to one of ordinary skill in the art at the time of invention that special purpose registers are present in the POWER architecture as disclosed by both Kahle and Davidian. The advantage of allowing a multiple load/store instruction access special purpose registers would have been to allow for a complete save and restore of processor state, including pertinent data stored in the special purpose registers. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize special purpose registers (omitted by Kahle) as disclosed by Davidian, in the environment disclosed by Kahle.

47. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kahle.

48. Regarding **claim 6**,

49. Kahle discloses the limitations as stated in **independent claim 1**.

50. Kahle does not explicitly disclose *the predetermined data transfer instructions* [being] *16-bit instructions.*

51. However, Kahle does not place a limitation on the size of the instructions utilized by the disclosed processor. Therefore, it would have been obvious to one of ordinary skill in the art at

the time of invention to utilize a standard instruction length common at the time of invention, such as a 16-bit instruction.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to George D. Zalepa whose telephone number is (571) 272-6754. The examiner can normally be reached on Monday-Friday (alt. Friday off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P. Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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